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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,944	11/07/2003	Gerard Boudon	FR920020012US1	2943

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EXAMINER	
WAI, ERIC CHARLES	

ART UNIT	PAPER NUMBER
2195	

MAIL DATE	DELIVERY MODE
07/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/605,944	BOUDON ET AL.	
	Examiner	Art Unit	
	Eric C. Wai	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7 are presented for examination.

Claim Objections

2. Claims 1-7 are objected to because of the following informalities: Figure elements in the claims.

3. Where possible, claims are to be complete in themselves. Incorporation by reference to a specific figure or table "is permitted only in exceptional circumstances where there is no practical way to define the invention in words and where it is more concise to incorporate by reference than duplicating a drawing or table into the claim. Incorporation by reference is a necessity doctrine, not for applicant's convenience." Ex parte Fressola, 27 USPQ2d 1608, 1609 (Bd. Pat. App. & Inter. 1993) (citations omitted). See MPEP § 2173.05(s).

4. Claim 7 is objected to because if the trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of the 35 U.S.C. 112, second paragraph. Ex parte Simpson, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or product. In fact, the value of a trademark would be lost to the extent that it became descriptive of a product, rather than used as an identification of a source or origin of a

product. Thus, the use of a trademark or trade name in a claim to identify or describe a material or product would not only render a claim indefinite, but would also constitute an improper use of the trademark or trade name. See MPEP 2173.05(u).

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms lack antecedent basis in the claims:

i. Claim 3, "said N Fields". It is unclear whether this is the same of different from the "N storage fields of claim 1".

b. The following terms are not clearly understood in the claims:

ii. Claim 1 lines 16-18 recites, "configured to store any valid task presented on said dedicated bus in parallel to all of said storage fields". It is unclear how the task is stored in parallel to all of the storage fields. Lines 6-9, the phrases "i.e." and "e.g." render the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

iii. Claim 5 lines 1-3 recites, "said second logic means enable said in all the free fields". It is unclear what the second logic means is enabling.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gilliland et al. (US Pat No. 4,229,790 hereinafter Gilliland).

9. Regarding claim 1, Gilliland teaches the improved FIFO based controller (12) for slave devices attached to the processor bus (14) of a CPU (11) for processing tasks and storing them in a FIFO memory, wherein a task consists of an address (Address) and its associated qualifying bits (ST, . . .), comprising:

first logic means (16,17) for enabling valid tasks, i.e. tasks having an address useful for at least one slave device, i.e. that will be followed by corresponding data and inhibiting others (e.g. "address only" tasks) to be presented on a dedicated bus (26); and (col 5 lines 4-8, wherein each PSW indicates an active status for that task),

a task management circuit (18) coupled to said first logic means comprising:

a FIFO memory (19) connected to said dedicated bus, provided with a plurality of N storage fields forming a pile, each field being identified by a determined address (Address0, . . .) and configured to store any valid task presented on said dedicated bus in parallel to all of said storage fields (col 5 lines 9-10).

10. Gilliland does not explicitly teach second logic means (21) that inhibit the writing of a task in the field (s) of the FIFO memory where a valid task has been entered and enable said writing in the first free field below in the pile. However, it is old and well known in the art to include logic to inhibit overwriting a valid entry.

11. Regarding claim 2, Gilliland teaches that the first logic means comprise:

a task detection circuit (16) coupled to the processor bus that detects valid tasks; and (col 5 lines 4-8, wherein active PSW pointers to the tasks are utilized).

12. Gilliland does not explicitly teach that the FIFO controller (17) coupled to said task detection circuit that generates an ADD TASK signal to add new tasks to be performed in said FIFO memory, a CLEAR TASK signal that clears all tasks therefrom that have been executed when said corresponding data are available on the processor bus, and a control signal that is applied to gating means (25) for only enabling said valid tasks to be presented on said dedicated bus.

13. However, Gilliland does teach that active tasks are placed on the FIFO buffer (col 5 lines 4-8). It would have been obvious to one or ordinary skill in the art at the time of the invention to include a signal to add and remove tasks from the FIFO memory. One would be motivated by the desire to signal the addition and removal of tasks for processing.

14. Regarding claim 3, Gilliland does not teach that a valid bit (V) stored in a register (27-x) is associated to each of said N fields, when it is set to a first binary value, this means that a valid task has been entered in the corresponding field.

15. It would have been obvious to one or ordinary skill in the art at the time of the invention to use a valid bit stored in a register for each of the fields. One would be motivated by the desire to lower the access latency by using register memory to determine whether a task is valid.

16. Regarding claim 4, Gilliland does not teach that the output of each pair of consecutive registers (27-0,27-1) is connected to the inputs of a two-way XOR gate (28-0), so that only one output of the N-1 XOR gates is active (at "1") indicating thereby the boundary between the field(s) of the FIFO memory where a valid task has been entered and the remaining free field(s).

17. It would have been obvious to one or ordinary skill in the art at the time of the invention to connect the output of the registers to a two-way XOR gate. It is well known in the art the XOR gate is a commonly used component in logic.

18. Regarding claim 5, Gilliland teaches that the second logic means (21) enable said in all the free fields of the FIFO memory instead of only the first free field (col 5 lines 4-10).

19. Regarding claim 6, Gilliland does not explicitly teach that a slave controller (20) coupled to said processor bus and task management circuit. It would have been obvious to one or ordinary skill in the art at the time of the invention to couple a slave controller to the processor bus and task management circuit. It is well known in the art that slave controllers are widely used in computer processing systems.

20. Regarding claim 7, Gilliland does not teach that the CPU is a 750 PowerPC microprocessor. It would have been obvious to one or ordinary skill in the art at the time of the invention to include that the CPU is a 750 PowerPC microprocessor. One would be motivated by the desire to extend the breadth of the claim by claiming a PowerPC microprocessor.

Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric C. Wai whose telephone number is 571-270-1012. The examiner can normally be reached on Mon-Thurs, 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng - Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EW

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